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by

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PRINCIPLES OF THE INTERWORKING OF THE CST-72 TELEMECHANICS SYSTEM CENTRAL STATION WITH THE MERA-302 MINICOMPUTER

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This paper presents the idea and the specific solution of the units that permit the link-up of the MERA-302 minicomputer with the CST-72 central station. The principles of information exchange between the two systems are described. The concept presented allows for the interworking of the CST-72 system with any type of machine adapted for real-time operation. The paper is a continuation of the cycle dealing with the application of CST-72 telemechanics at the Municipal Gas Management in Warsaw [3].

The configuration shown in Figure 1 shows the arrangement of systems adopted for realizing the interworking of the CST-72 system central station with the MERA-302 minicomputer. The basic elements are the CST-72 central station interface and the control unit of the MERA-302 computer.

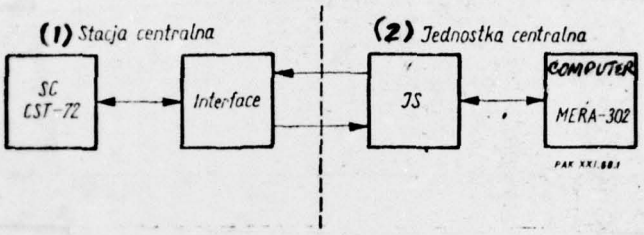

Figure 1. Link-up of the CST-72 central station with the MERA-302 minicomputer.

Key: (1) central station; (2) central unit

CST-72 Interface Unit

The task of the unit is to act as a mediator in the two-way exchange of information between the MERA-302 (henceforth called the JC) and all other systems of the central station. Information exchange occurs through the buffer registers in the interface. The exchange is controlled by the JC central unit which addresses the input and output channels. The additional task of the unit is to permit testing (from the front plate of the interface panel) of all external systems by means of addresses and information given by switches. The interface can interwork with the JC with a word length of 8, 12, or 16 bits; the shortest word (8 bits) determines the interface structure.

The block diagram of the interface is shown in Figure 2.

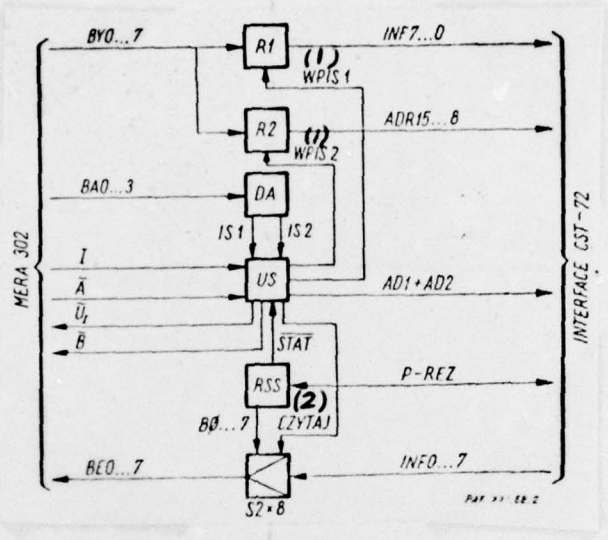

Figure 2. Block diagram of the CST-72 central station interface system.

Key: (1) write-in; (2) read

A distinction is made between the addresses of external devices transmitted from the JC through the address register of interface RW_b to the devices, and specific information transmitted from the JC through the RW_a register and to the JC through the register RW_c. The signals of the address register RW_b and the information register RW_a are designated jointly 15.....0 as a single 16-bit word. The division into an address and information part is not fixed; the word configurations vary for different external devices. However it is always true that at least the three highest-order bits refer to the address. With a 16-bit machine word length the registers RW_a and RW_b can be considered as a single 16-bit register with a parallel input controlled by signal AD1 +AD2.

The address information written into the registers is decoded in decoders DAJ for the purpose of creating the following address groups:

(1) F7.....F0
(2) F7...M0
(3) N3...N0
(4) P3...P0

The group of address signals F7...F0 is gated by pulse F. As a result of this in the address devices the signals F7..F0 play the role of pulses with respect to the longer lasting (static) signals of groups M, N, and P.

The following devices are used when information is transferred to the JC:

- --buffer register RW_C
- a two-stage gated logical adder which allows the selection of one 8-bit word from the 10
- -two buffer registers R1 memorizing calls from external devices.

The operation of the devices is based on the principle that address signals M and N are selected in module Σ1 according to the word supplied at the input of buffer register RW_C , and pulse F7 enters the word into the register. The write-in into the RW_C and the transfer from the RW_C to the JC are separate operations in the JC program.

Call signals of external devices are memorized in registers R1. For call identification the states of registers R1 are entered into the JC through register RW_C .

Module USI comprises the control system generating signals that control the operation of individual modules.

The state of the buffer registers can be reproduced during testing by means of control lamps; the signals of the register states are amplified in modules W-200.

Control Unit

The task of the control unit (henceforth called the JS) is to assure the interworking between the interface devices of the JC arithmometer channel and the interface devices of the CST-72 central station.

The JS communicates with the interface unit of the JC arithmometer channel by means of an 8-bit machine word; it has sent a 16-bit word to the SC interface unit, collecting an 8-bit word from it. The JS can control many operations simultaneously that are not connected with data transmission; but, it can control only one data transmission operation.

Figure 3 shows the block diagram of the JS.

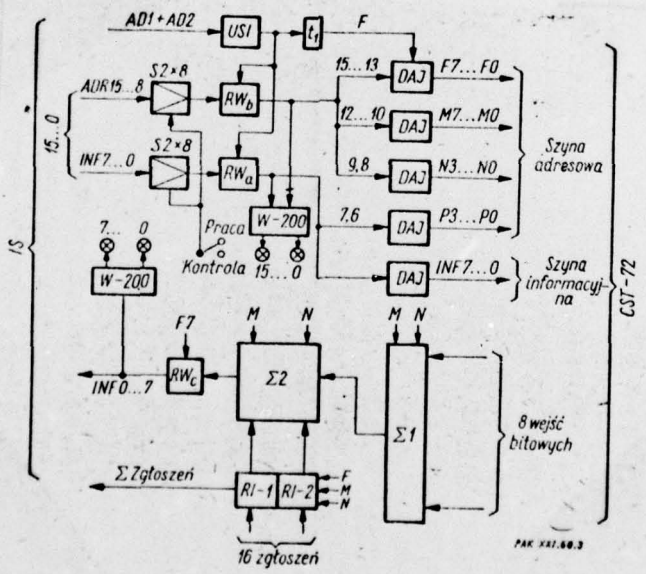

Figure 3. Block diagram of the control unit of the MERA-302 minicomputer.

Key: (1) address bus; (2) information bus; (3) 8 imput bits; (4) 16 calls; (5) Σ calls; (6) operation; (7) control

Information Transfer

There are two operations in the transfer of information from the JC to the SC. First of all it is necessary to write in, from bus BY0..7 to buffer register R1 the information word INF7..0. On bus BA0..3 appears the first JS address. After decoding in the decoder of address DA pulse JS1 is generated. The appearance of pulse JS1 when the instruction PISZ ZNAK (A) [WRITE SIGN], the signal STAT, and the strobing pulse I are present generates in the control system US the write-in signal WPISI1 which writes the information word into the buffer register R1.

Next it is necessary to write in, also from bus BY0...7, the address word ADR15...8 into register R2. On bus BA0 ..3 appears a second JS address.

After decoding In the decoder of address DA pulse JS2 is generated. The appearance of pulse JS2 in the presence of the instruction PISZ ZNAK (A), signal STAT, and strobing pulse I generates in the control system US the pulse WPIS 2. Pulse WPIS 2 writes the address word into buffer register R2. The rear slope of pulse WPISZ 2 generates, through the US control system, the signal AD1 +AD2 which rewrites the 16-bit word from both buffer registers R1 and R2 into buffer registers RW_a and RW_b of the SC interface unit.

Information Gathering

There are also two operations when information is collected from the SC into the JC. First of all, in the same way as earlier described, the address of the device ADR15..8 from which information is to be collected is sent to the SC. The information is written into the buffer register RW_c of the SC interface unit and appears on the input busses of the JS as INF0...7.

Next, the first address of the JS appears on busses BA0...3. After decoding In the decoder of address DA, pulse JS1 is generated.

The appearance of pulse JS1 when the instruction CZYTAJ ZNAK (A) [READ SIGN] and the signal STAT are present creates in the control system US the signal CZYTAJ [READ] and its being sent to the adder S2x8. The signal CZYTAJ causes information INF0..7

to be sent to the output busses of the JS BEO...7.

Word of the State

The JS creates the word of the device's state with an 8-bit length, which reflects the actual state of the control unit. Separate bits of the word of state are connected with devices in the JS which the JC channel must be informed about. The word of state is created in the register of the word of state of the RSS. The following positions in the register of the word of state account for individual events.

Position 0: BN-the central station is inoperative (tested from the back-up system). This position is established by the front of pulse P-REZ (Fig 3) coming from the SC, and set to zero by the rear slope of the same pulse.

Position 1: BZ-JS is inoperative (is in the process of executing a transmission initiated through the channel). This position is established by pulse WPIS1 or WPIS2, and set to zero by instruction PISZ ZNAK.

The remaining positions of the word of state are constantly made zero. The situation when individual positions of the word of state take on value "1" can be signaled using interrupt U_I. The channel is informed by line B when there is a non-zero word of state.

Final Considerations

The control unit described has been developed and mounted in the JS panel of the MERA-302 minicomputer. The use of the system for several months has confirmed the correctness of the adopted solutions for using intermediary systems in the transfer of information between the MERA-302 computer and the CST-72 system central station.

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